Reconfigurable Communication Silicon IP Design for Multi-spec/Multi-mode Communication Systems

Prof. An-Yeu (Andy) Wu

Graduate Institute of Electronics Engineering and

Department of Electrical Engineering

National Taiwan University (NTU), Taipei, Taiwan

Spec of LDPC Codes in IEEE 802.16e

- Dimension of Base matrix : 12*24
- Code rate (R) : 1/2
- Expanding factor : p = 24, 28, ..., and 96
- Number of cyclic-shifted bits : $s(p,i,j) = [\frac{s(i,j) * p}{96}]$
- Parity check matrix :

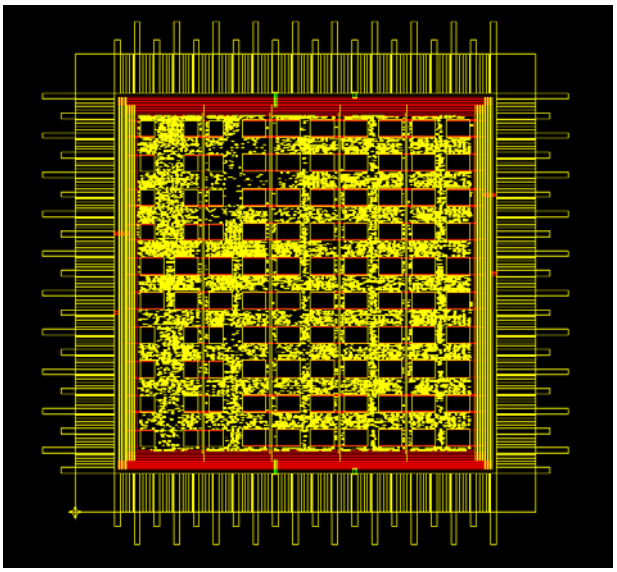
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1		94	73						55	83			7	0										
2		27				22	79	9				12		0	0									
3				24	22	81		33				0			0	0								
4	61		47						65	25						0	0							
5			39				84			41	72						0	0						
6					46	40		82				79	0					0	0					
7			95	53			A			14	18		B					T	0	0				
8		11	73				2			47										0	0			
9	12				83	24		43				51									0	0		
10						94		59			70	72										0	0	
11			7	65					39	49													0	0
12	43					66		41				26	7											0

C D E

(19 kinds of code-size)

N(bits)	N(bytes)	K(bytes) R=1/2
576	72	36
672	84	42
768	96	48
864	108	54
960	120	60
1056	132	66
1152	144	72
1248	156	78
1344	168	84
1440	180	90
1536	192	96
1632	204	102
1728	216	108
1824	228	114
1920	240	120
2016	252	126
2112	264	132
2208	276	138
2304	288	144

Multi-mode Chip Summary



Published in IEEE Journal of Solid-State Circuits (JSSC), Feb. 2008

Irregular LDPC codes with Code Rate ½ (19 Kinds of operating mode)	
Cell Library	TSMC 0.13um 1P8M
Work Voltage	1.2 V / 3.3 V
Gate Count	393 K
Core Size	2.11mm x 2.11mm
Die Size	2.88mm x 2.88mm
Operating Frequency	100 MHz
Power Consumption	62mW

# of Single-Port Register file	24 (96*8)
# of Two-port Register file	76 (96*8)

工業技術研究院
Industrial Technology Research Institute

Overview of ITRI's Parallel Architecture Core (PAC) DSP Project

Dr. An-Yeu (Andy) Wu

Deputy General Director
SoC Technology Center (STC)
Industrial Technology Research Institute (ITRI), Taiwan

工業技術研究院
Industrial Technology
Research Institute

Outline

- Introduction
- Parallel Architecture Core (PAC) DSP Core
- PAC SoC Platform with DVFS Feature
- PAC Phase-II Project (PAC-II)
- Conclusion

工業技術研究院
Industrial Technology
Research Institute

History of SoC Technology Center (STC) in ITRI

UMC (1980)

tsmc (1986)

EOL (formerly ERSO)

PMD
(Personal Media Device)

ICL

South ITRI

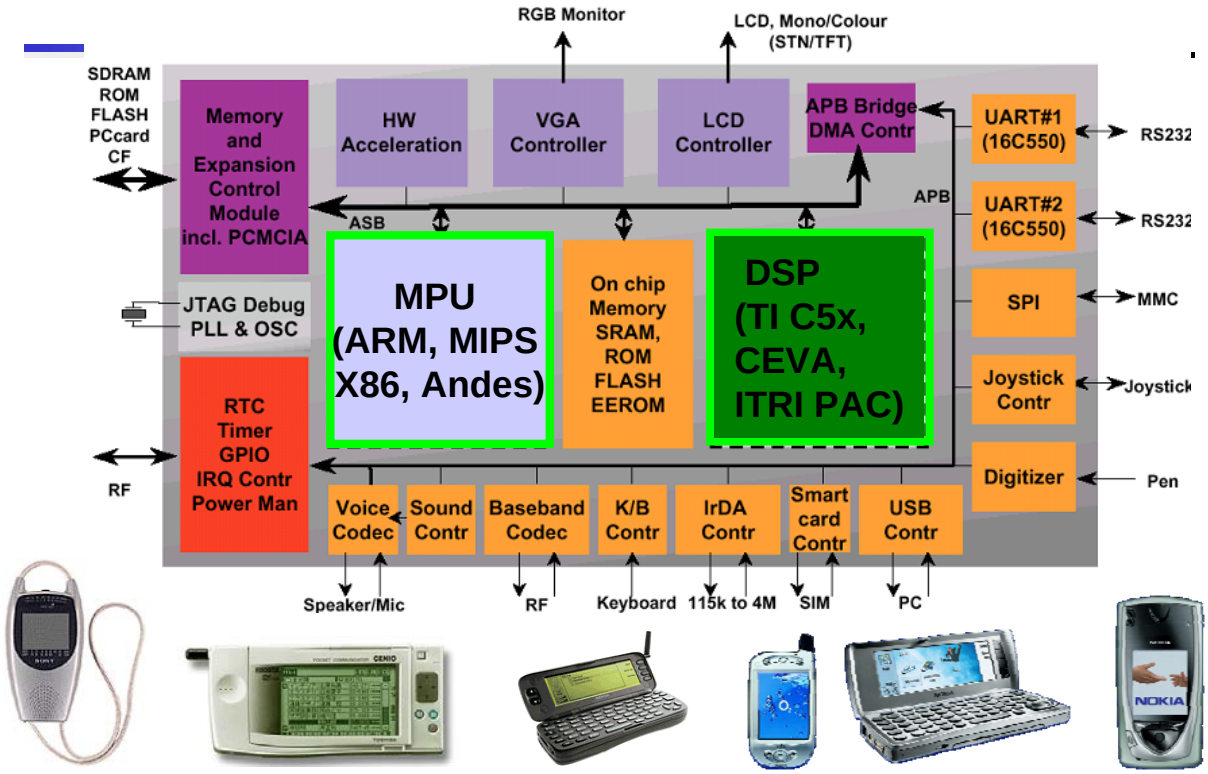
SoC Technology Center (STC)
(founded: 2000)

ICL (formerly CCL)
Founded :1990)

- **Lead/coordinate ITRI-WiMAX Project!**
- RF/AMS Circuits、PAC DSP Processor & SoC Platform
- MIMO Mobile WiMAX Technologies
- WiMAX-enabled PMD

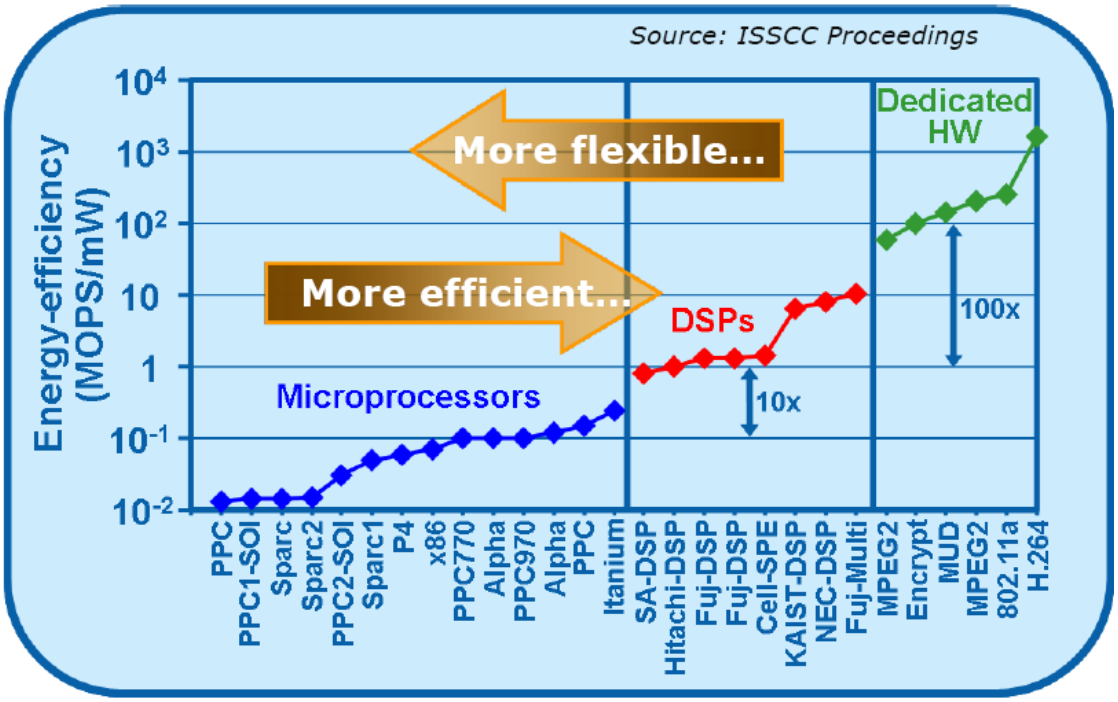
工業技術研究院
Industrial Technology Research Institute

Modern SoC Platform



工業技術研究院
Industrial Technology Research Institute

Flexibility & Energy Efficiency



工業技術研究院
Industrial Technology Research Institute

Industry Status and Need!

- *We need Programmable DSP Solution in Internet Era!*

工業技術研究院
Industrial Technology Research Institute

Compression Formats (wiki)

Video compression formats	**ISO/IEC**	**ITU-T**	**Others**
	MJPEG · MPEG-1 · MPEG-2 · MPEG-4 ASP · **MPEG-4/AVC**	H.261 · H.262 · H.263 · **H.264**	AVS · Bink · Dirac · Indeo · MJPEG · RealVideo · Theora · VC-1 · VP6 · VP7 · WMV
Audio compression formats	**ISO/IEC**	**ITU-T**	**Others**
	MPEG-1 Layer III (MP3) · MPEG-1 Layer II · MPEG-1 Layer I · AAC · HE-AAC · HE-AAC v2 · aacPlus v2	G.711 · G.722 · G.722.1 · G.722.2 · G.723 · G.723.1 · G.726 · G.728 · G.729 · G.729.1 · G.729a	AC3 · Apple Lossless · ATRAC · FLAC · iLBC · Monkey's Audio · μ-law · Musepack · Nellymoser · RealAudio · SHN · Speex · Vorbis · WavPack · WMA · TAK
Image compression formats	**ISO/IEC/ITU-T**		**Others**
	JPEG · JPEG 2000 · lossless JPEG · JBIG · JBIG2 · PNG · WBMP		APNG · ICER · MNG · BMP · GIF · ILBM · PCX · PGF · TGA · TIFF · HD Photo
Media container formats	**General**		**Audio only**
	3GP · ASF · AVI · DMF · DPX · FLV · Matroska · MP4 · MXF · NUT · Ogg · Ogg Media · QuickTime · RealMedia · VOB		AIFF · AU · WAV

http://en.wikipedia.org/wiki/H.264

工業技術研究院
Industrial Technology
Research Institute

DSP SoCs: NRE and Cost

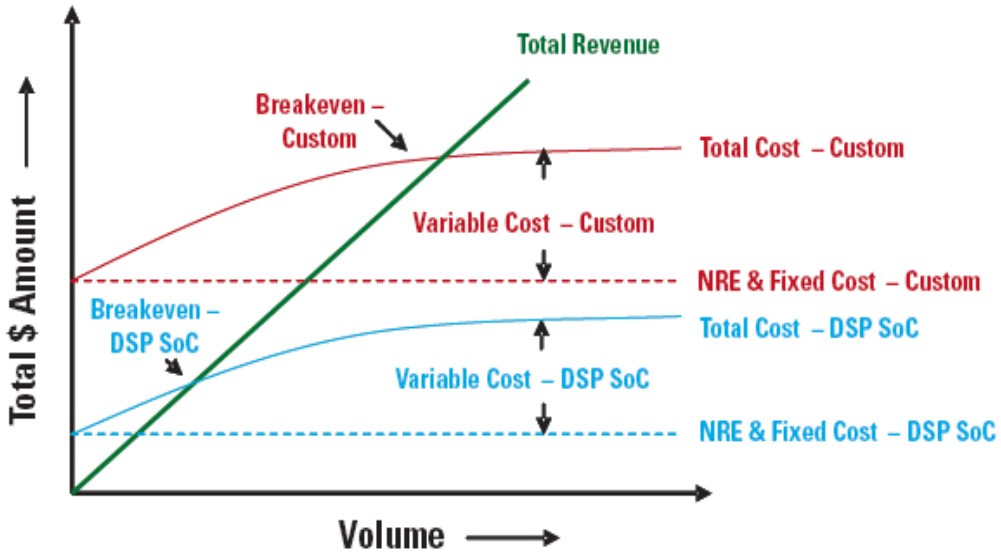


Figure 3: Standardized DSP SoCs Lower NRE and Fixed Cost

Source: TI C6x DSP datasheet

工業技術研究院
Industrial Technology
Research Institute

Outline

- Introduction
- Parallel Architecture Core (PAC) DSP Core
- PAC SoC Platform with DVFS Feature
- PAC Phase-II Project (PAC-II)
- Conclusion

工業技術研究院
Industrial Technology Research Institute

Parallel Architecture Core (PAC) DSP chronogram

2004.6

DSP Flow Performance Evaluation

PAC DSP v1.5

Freq: 200MHz
Power: N/A
0.13 μ m

MP3 Demo!!

2005.6

Portable Media Player

PAC DSP v2.0

Freq: 250MHz
Power: 1.5mW/MHz
0.13 μ m (AP)

Newly Added Features

- Customized FU Interface
- Embedded ICE
- Gated Clock, Multiple Vth & Low-power Clock Tree Synthesis
- Power Management (Multi-Frequency)

2007.1

Smart Phone

PAC DSP v3.0

Freq: 300/350MHz
Power: 1 mW/MHz
90nm Tape-out ready

Newly Added Features

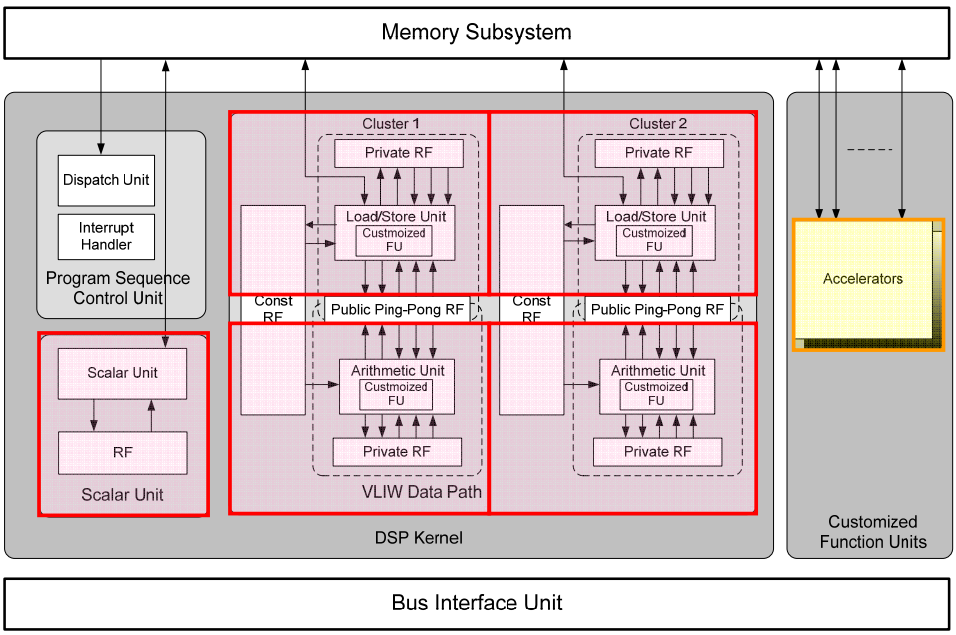
- Power Management (DVS/DFS)
- Optimized Memory Subsystem

H.264 Decoder
VGA Demo @30fps!!

工業技術研究院
Industrial Technology Research Institute

PAC DSP Kernel

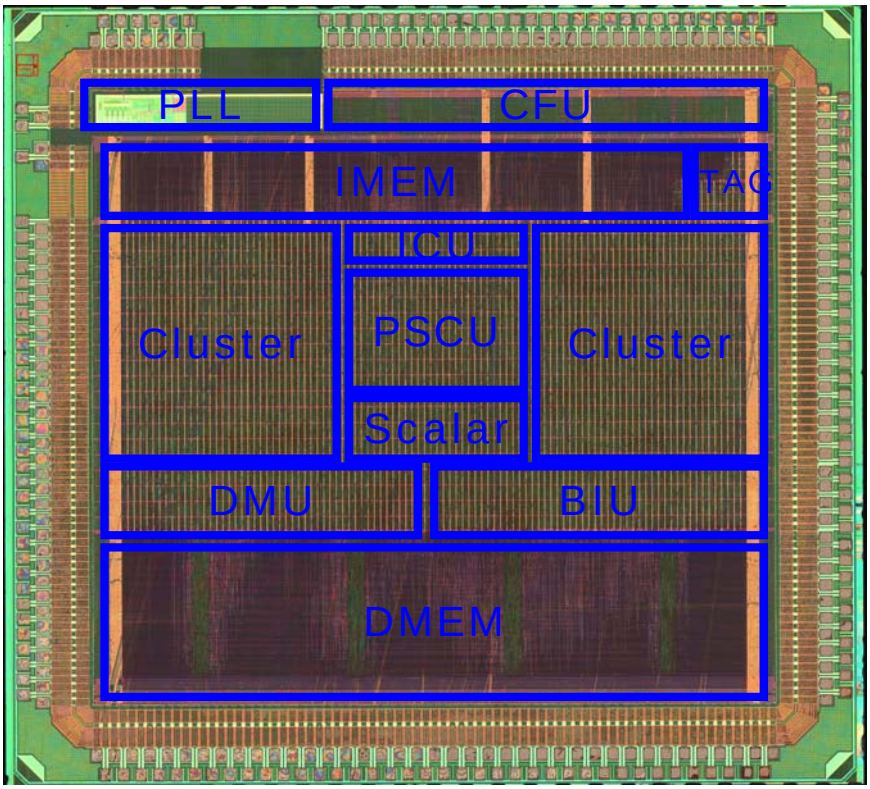
- 5-way VLIW with Customized Function Units



Copyright ITRI 工業技術研究院

工業技術研究院
Industrial Technology
Research Institute

STC PAC-I DSP



工業技術研究院
Industrial Technology
Research Institute

PAC DSP3.0 DSP Kernel Benchmarks

DSP Platform	PACDSP 3.0	ADI BF5xx	CEVA-X 1620	CEVA-X 1640	LSI ZSP500	StarCore SC1200	StarCore SC1400	TI C5501	TI C6414
	300MHz	750MHZ	450MHZ	340MHZ	340MHZ	305MHZ	300MHZ	300MHZ	1000MHZ
Architecture	5-way VLIW 2MACs	1-issue dual MAC	8-way VLIW 2 MACs	8-way VLIW 4 MACs	4-issue Superscalar	4-way VLIW 2 MACs	6-way VLIW 4 MACs	1-issue dual MAC	8-way VLIW
Vector Add	21	40	33	18	25	19	19	47	27
Vector Dot	23	29	26	19	22	25	16	43	25
Vector Max	43	35	29	22	32	44	27	45	36
Control	444	758	639	639	382	425	425	1012	475
Bit unpack	146	408	106	61	166	164	124	251	97
Real-vauledBlock FIR	317	381	351	182	355	354	185	394	194
Complex-vauledBlock FIR	993	1380	1330	690	1301	1333	675	1409	674
SS FIR	18	23	21	19	20	16	14	25	26
IIR	19	16	9	8	11	10	9	16	16
LMS	34	45	29	24	32	26	19	57	37
Viterbi	3505	6067	2304	1925	3249	2880	1935	6690	1740
FFT	1684	2632	2207	1248	2323	3230	1631	4922	1246

- (Cycle counts: Submitted for certification and subject to change)
- **4 benchmarks NO.1, 5 benchmarks NO.2, 3 benchmarks NO.3**
- **Compared Targets: CEVA-X 1620, Star Core SC1200**

工業技術研究院
Industrial Technology Research Institute

STC PAC DSP No.1 Index

Vender Property	ITRI/STC	StarCore		CEVA
	PAC DSP	SC2000 (SC2400)	SC1200 (SC1400)	CEVA-X 1620
Architecture	5 way VLIW	6 way VLIW	6 way VLIW	8 way VLIW
Frequency (MHz)	312	250~350	305	450
Process	0.13μm	0.13μm~90nm	0.13μm	0.13μm
Performance (MIPS)	1560	1500~2100	1830	3600
Power Consumption* (mW/MIPS)	0.08	-	0.098	0.08
Power Consumption* (mW)	124.8 No. 1	-	179.34	288
Area	1.2mm^2 No. 1	-	-	1.6 mm^2
Power Management	Yes	Yes	Yes	Yes

*Without Memory
**350K Gates

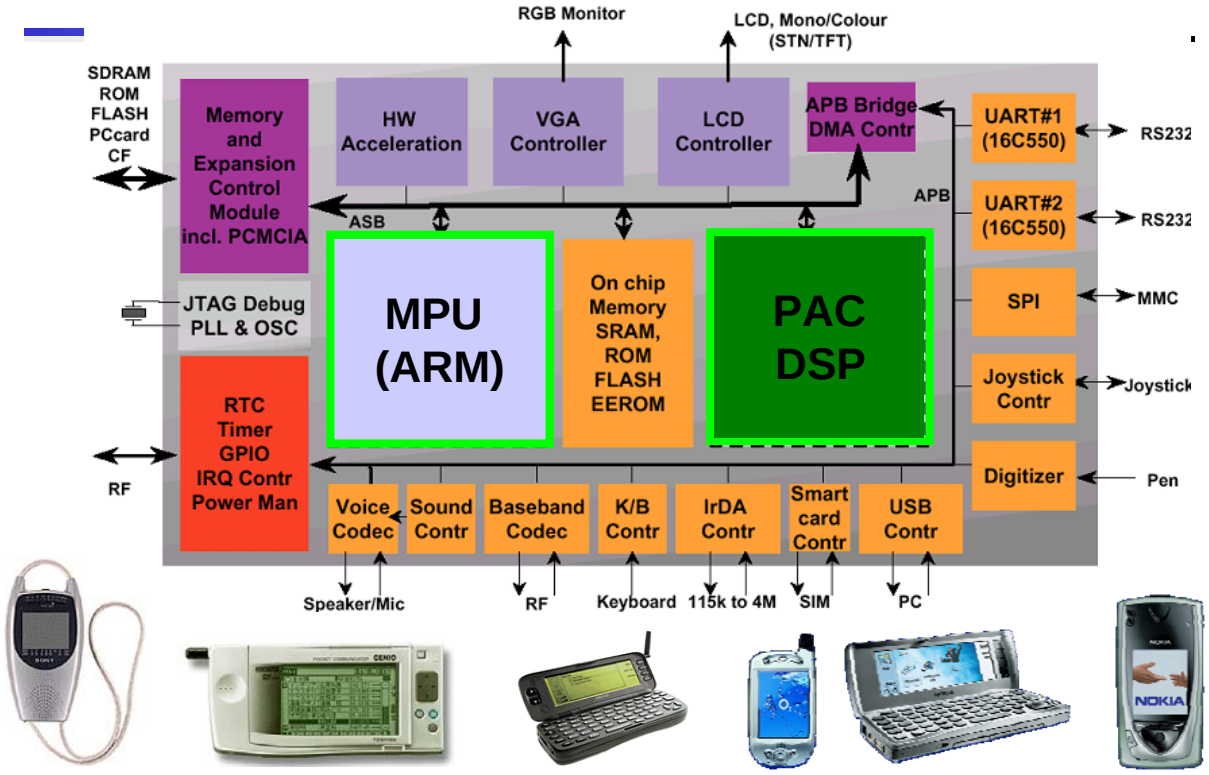
工業技術研究院
Industrial Technology Research Institute

Outline

- Introduction
- Parallel Architecture Core (PAC) DSP Core
- PAC SoC Platform with DVFS Feature
- PAC Phase-II Project (PAC-II)
- Conclusion

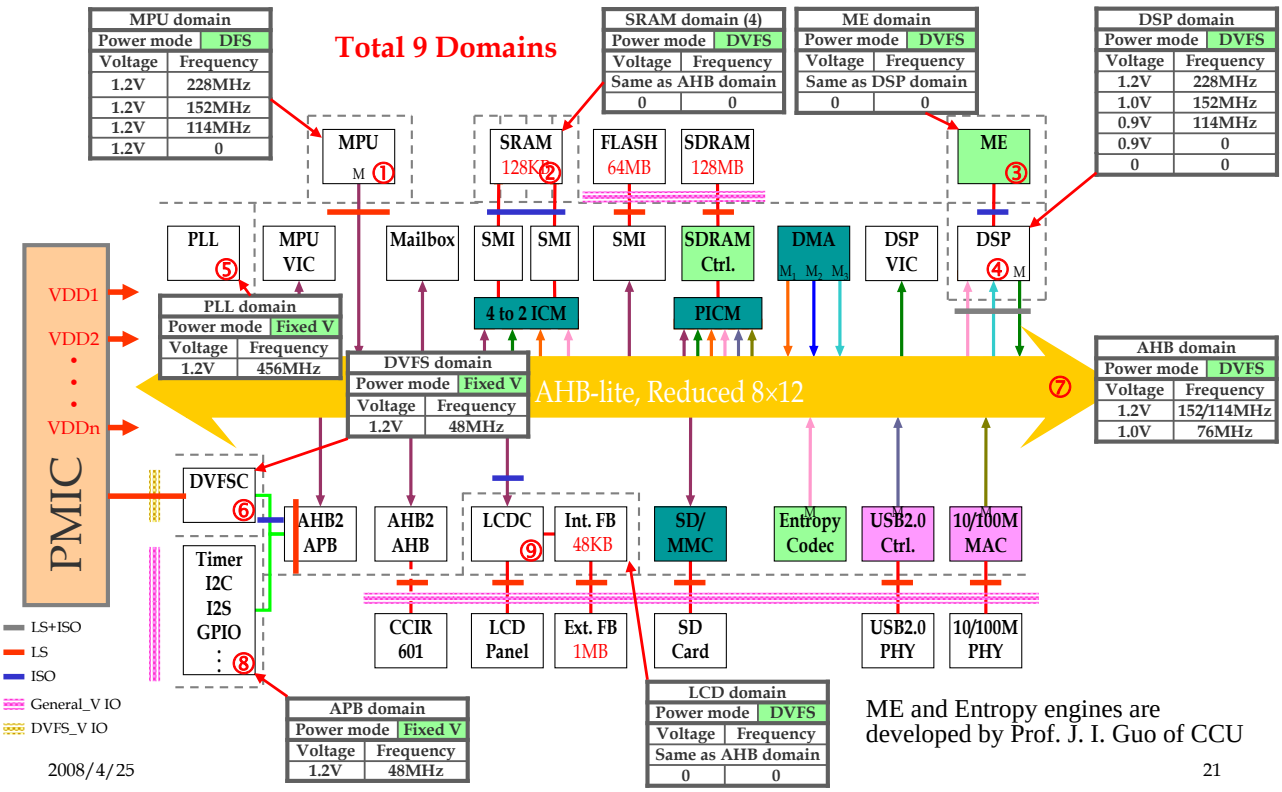
工業技術研究院
Industrial Technology Research Institute

Under the Hook of MID/GPhone: PxD SoC Platform



工業技術研究院
Industrial Technology Research Institute

PAC Solo with Dynamic Voltage and Frequency Scaling (DVFS)



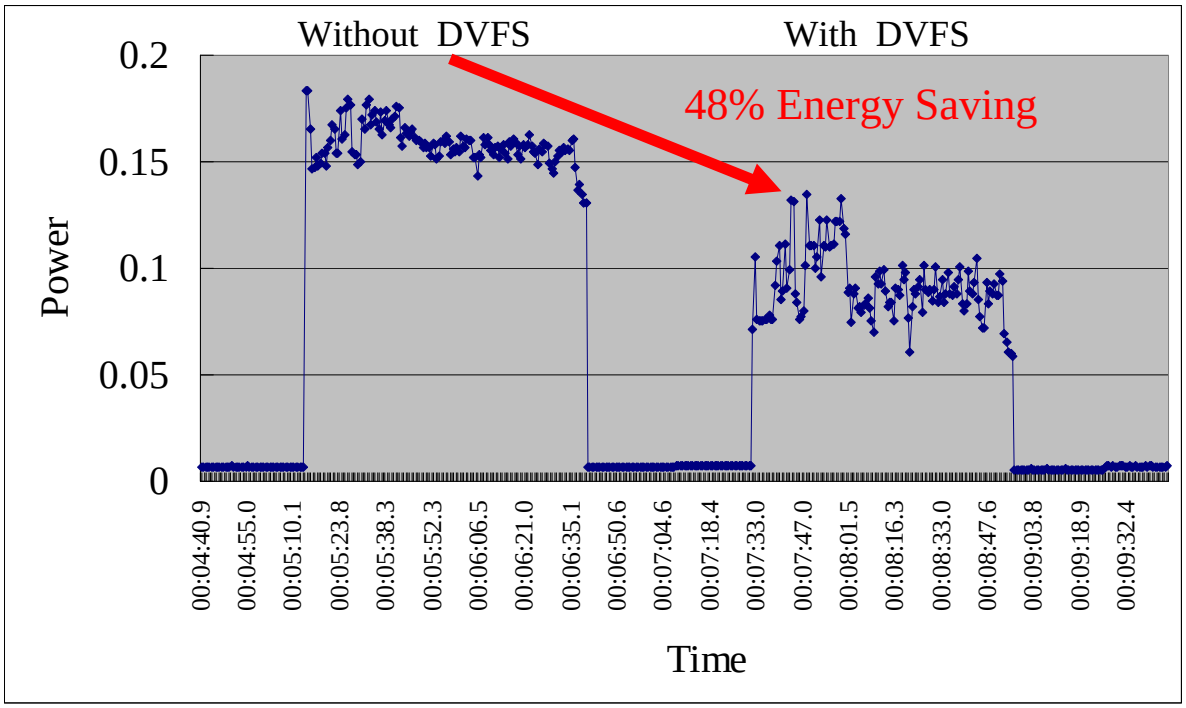
ME and Entropy engines are developed by Prof. J. I. Guo of CCU

工業技術研究院
Industrial Technology
Research Institute

Power Domains of PAC SoC

Power domain name	Power modes	Operation condition		Individual power down
		Voltage	Frequency	
MPU-domain	Active-1	1.2V	228MHz	N
	Active-2	1.2V	152MHz	
	Active-3	1.2V	114MHz	
	Inactive	1.2V	0	
DSP-domain	Active-1	1.2V	228MHz	Y
	Active-2	1.0V	152MHz	
	Active-3	0.9V	114MHz	
	Inactive	0.9V	0	
	Sleep	0	0	
ME-domain	Same as DSP-domain			Y
AHB-domain	Full-speed	1.2V	152/114MHz	N
	Low-power	1.0V	76MHz	
SRAM-domain, LCD-domain	Same as AHB-domain			Y
APB-domain, DVFS domain	Fix V	1.2V	48MHz	N
PLL-domain	Fix V	1.2V	456MHz	N

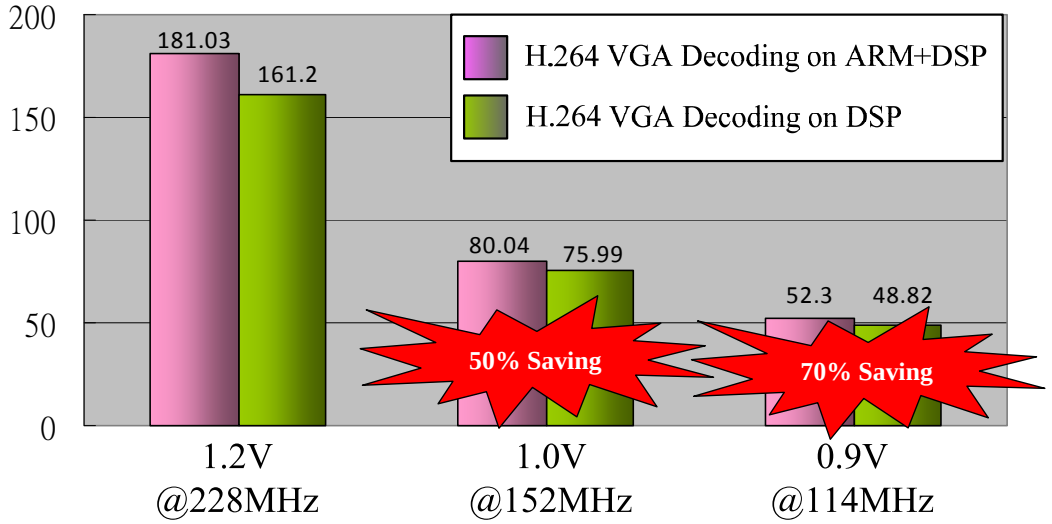
工業技術研究院
Industrial Technology
Research Institute



Figures during H.264 Decoding (real-time data shown on PC Screen)

工業技術研究院
Industrial Technology Research Institute

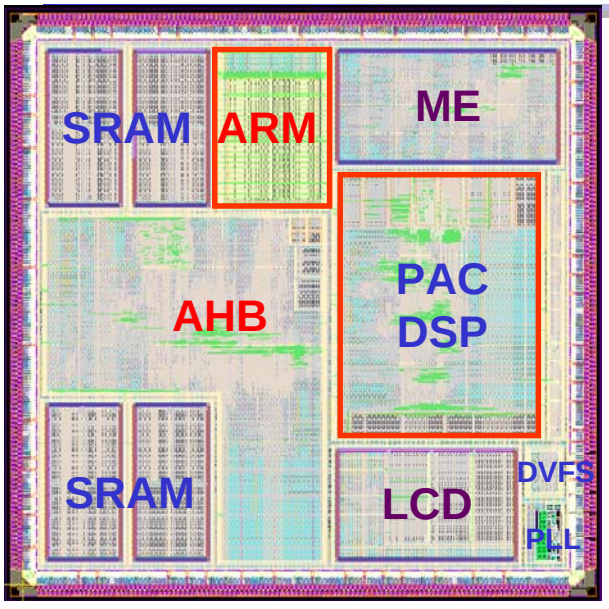
PAC DSP Power Consumption (mW)



PAC DSP Voltage & Frequency

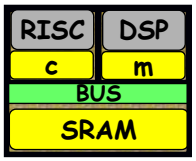
工業技術研究院
Industrial Technology Research Institute

PMP Dual-core SoC by ITRI/STC



Process	TSMC 0.13μm CMOS Logic 1P8M Salicide 1.2V/2.5V
Frequency	ARM 228MHz
	DSP 228MHz
	AHB 114MHz
	APB 48MHz
Package	BGA
Voltage	1.2V/2.5V
Chip Size	9,991x10,000μm²
Gate Count	1,169K (w.o. ARM, SRAM & PLL)

TI OMAP Style

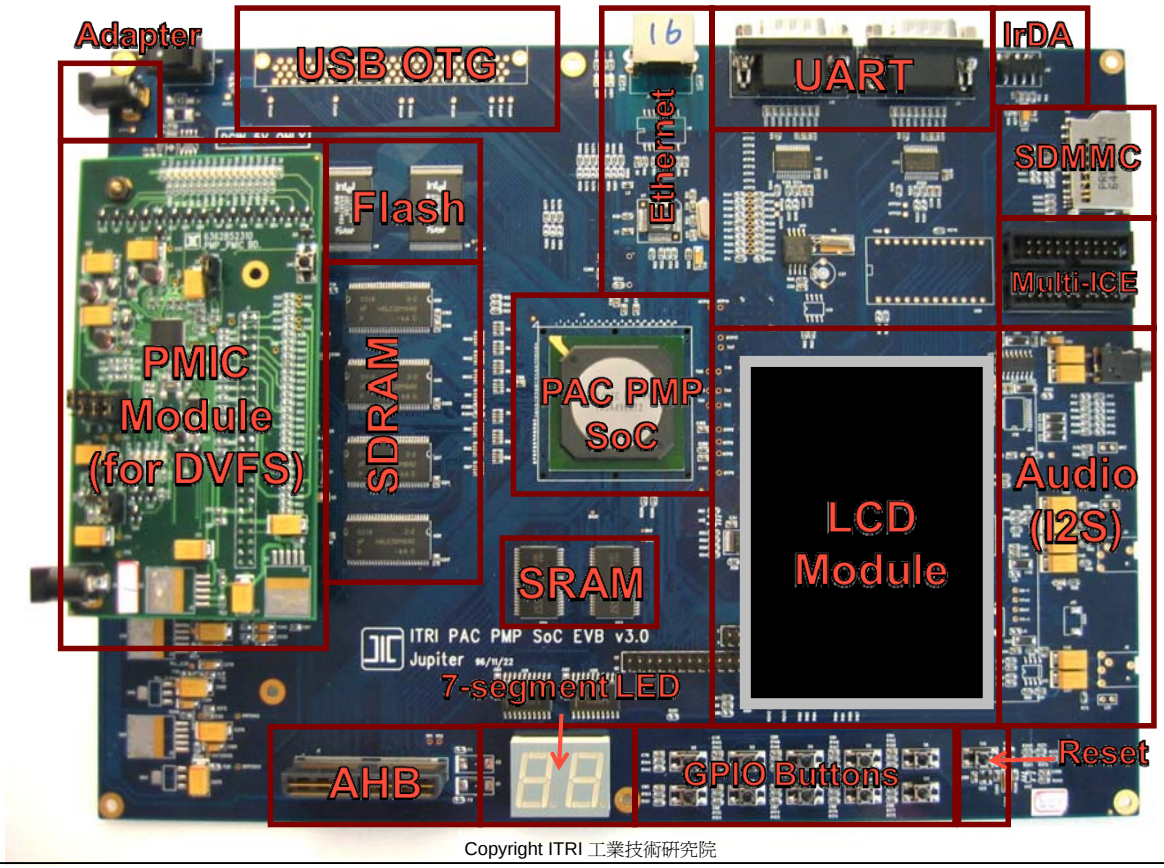


Taiwan's first low-power/high performance DSP and Dual-core multimedia processor platform

(PAC DSP & PAC Platform)

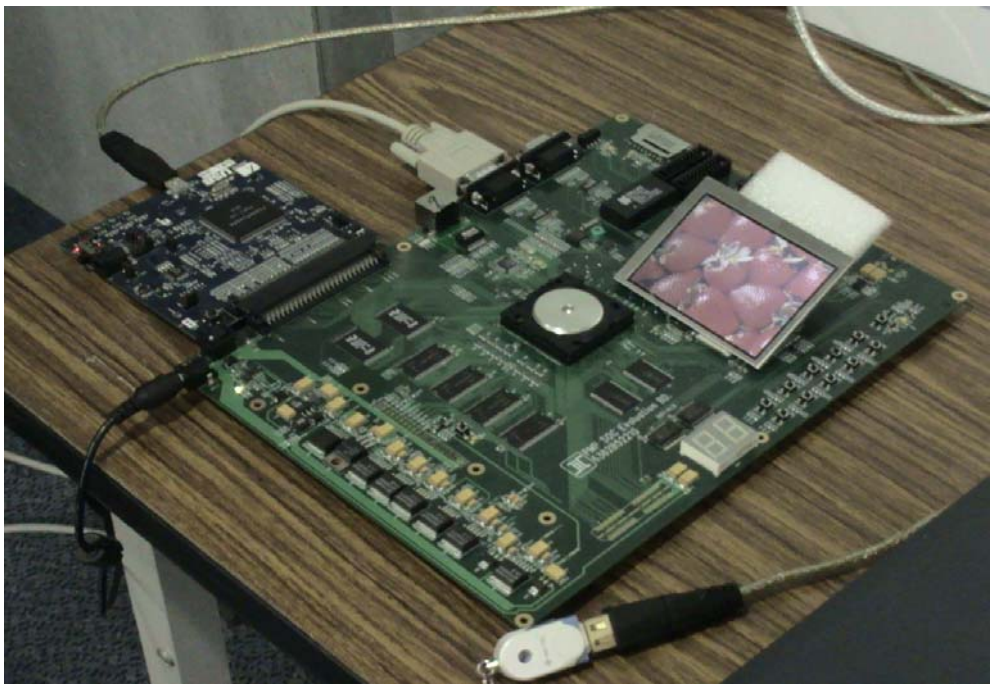
工業技術研究院
Industrial Technology Research Institute

PMP SoC (ARM+PACDSP) Platform



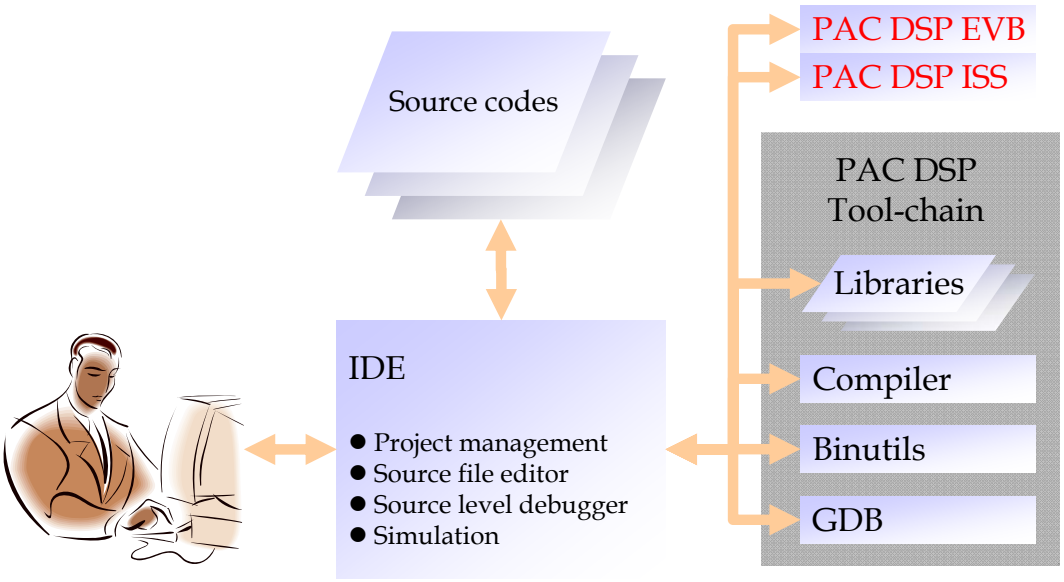
工業技術研究院
Industrial Technology Research Institute

PMD SoC (ARM+PAC) Platform Running H.264



工業技術研究院
Industrial Technology
Research Institute

Integrated Development Environment (IDE) for PACDSP



Tool-chain and IDE are developed by Prof. J. K. Lee of NTHU

工業技術研究院
Industrial Technology
Research Institute

Codec Menu for PACDSP

- Multimedia Codec
  - H.264 decoder：ISO 14496-10 MPEG-4/AVC
  - WMV decoder ：SMPTE 421M-2006 simple
  - MPEG-2 decoder：MPEG-2 (13817-2) main
  - JPEG codec：T.81 baseline interlace
  - AAC codec：MPEG-2 AAC (13818-7) low complexity
  - WMA decoder：WMA-7

工業技術研究院
Industrial Technology Research Institute

PAC PMP Sales Package

PAC PMP EVB

DSP ICE

PMIC Module (for DVFS)

Power Line

User Guides & BSP CD

工業技術研究院
Industrial Technology Research Institute

PAC – Parallel Architecture Core
PACDSP + PAC Platform

PACDSP
- Low-Power High-Performance DSP

PAC Platform
- Multimedia Processor SoC for Mobile Devices (PMP SoC)

DSP Features
- Scalable VLIW Datapath
- Variable-Length Instruction/Packet
- Distributed & Ping-pong Register File
- Dynamic Power Management
- Customized Instruction Set
- Coprocessor Interface

SoC Features
- Scalable Performance
- Dynamic Voltage & Frequency Scaling (DVFS)
- Rich Codec for Multimedia Applications
- Peripherals and I/O ready

Technical Spec
- Process : 130 nm/ 90 nm
- Frequency : 300 ~ 450MHz
- Performance : 1200 ~ 2000 MMACs, 1500MIPS
- Power Consumption : ~0.08mW/MIPS

工業技術研究院
Industrial Technology
Research Institute

Outline

- Introduction
- Parallel Architecture Core (PAC) DSP Core
- PAC SoC Platform with DVFS Feature
- PAC Phase-II Project (PAC-II)
- Conclusion

工業技術研究院
Industrial Technology
Research Institute

I. Enhanced PACDSP Family

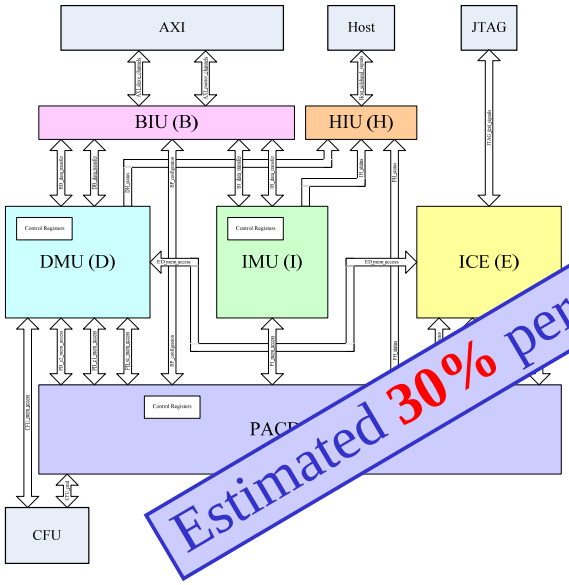
- V3 (**PAC-VLIW**) — Ready
  - V3.2
    - Original design with IP consolidation
    - Ready for sale/transfer
  - V3.3 (**PAC-*plus!***)
    - AMBA AXI-support
    - Configurable system interfaces with automatic application-specific customization tool (based on ESL technology)

- V4 (**PAC-*lite***) — Ongoing
  - Digital audio & ultra-low voltage/power applications
- V5 (**PAC-SIMD**) for Multicore Structure
  - Improved performance & energy efficiency

工業技術研究院
Industrial Technology
Research Institute

PAC-*plus!* (*v.3.3*)

AXI (AMBA 3.0)



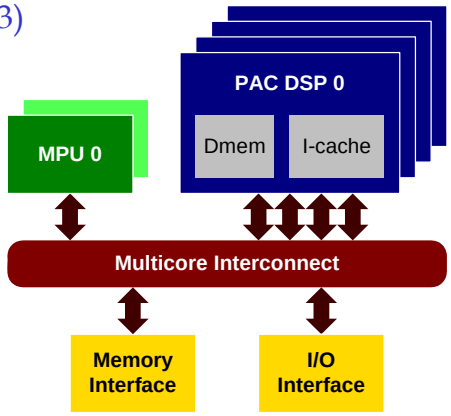
Estimated 30% performance improvement

- Instruction Memory U… (IMU)
  - Configurable a… scratchpad
  - Subsettabl… …es
  - AX… …che controller
- D… …mory Unit (DMU)
  - …arallel banks with individual power modes
  - Four ports with programmable priorities
  - DSP-enhanced DMA controller
- Bus Interface Unit (BIU)
  - AXI-support (AMBA 3.0)
  - Asynchronous FIFO-support

工業技術研究院
Industrial Technology
Research Institute

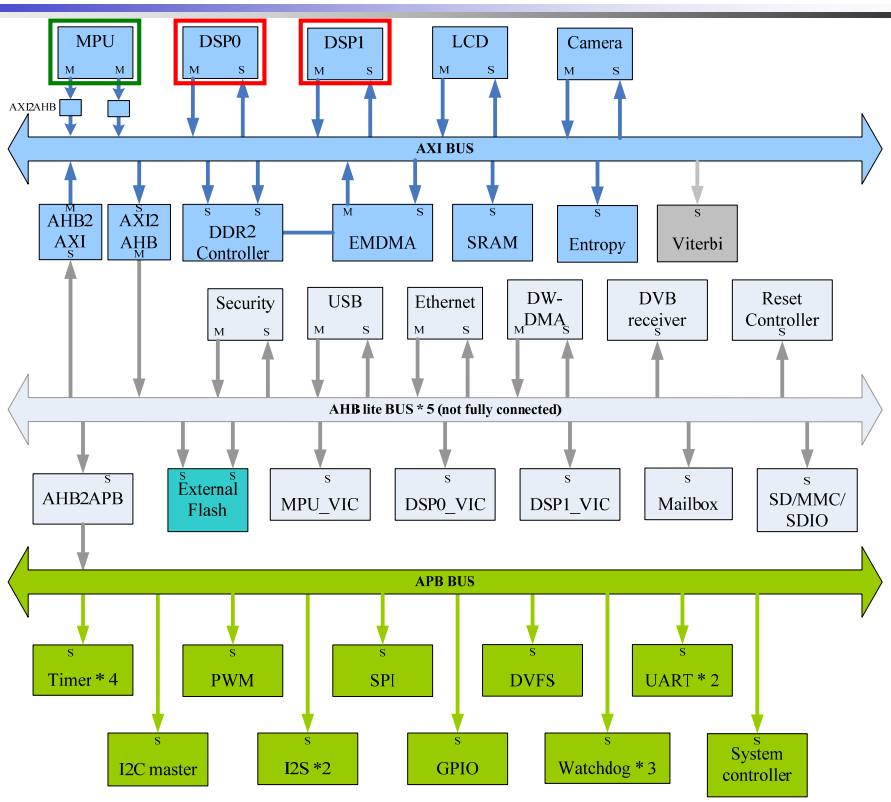
PAC I & PAC II

- PAC I (2004~2007)
  - 1 × MPU + 1 × **PAC-VLIW** (PACDSP V3)
  - **PAC Solo** (PMP SoC)
    - ARM922T + PACDSP V3.0
- PAC II
  - *k* × MPU +
    n × **PAC-VLIW** (PACDSP V3) +
    m × **PAC-*lite*** (PACDSP V4) +
    l × **PAC-SIMD** (PACDSP V5)
  - **PAC Duo (2008)**
    - ARM926 + 2 × PAC-*plus!* (PACDSP V3.3; **PAC-VLIW**)
  - **PAC Quad (Planning)**



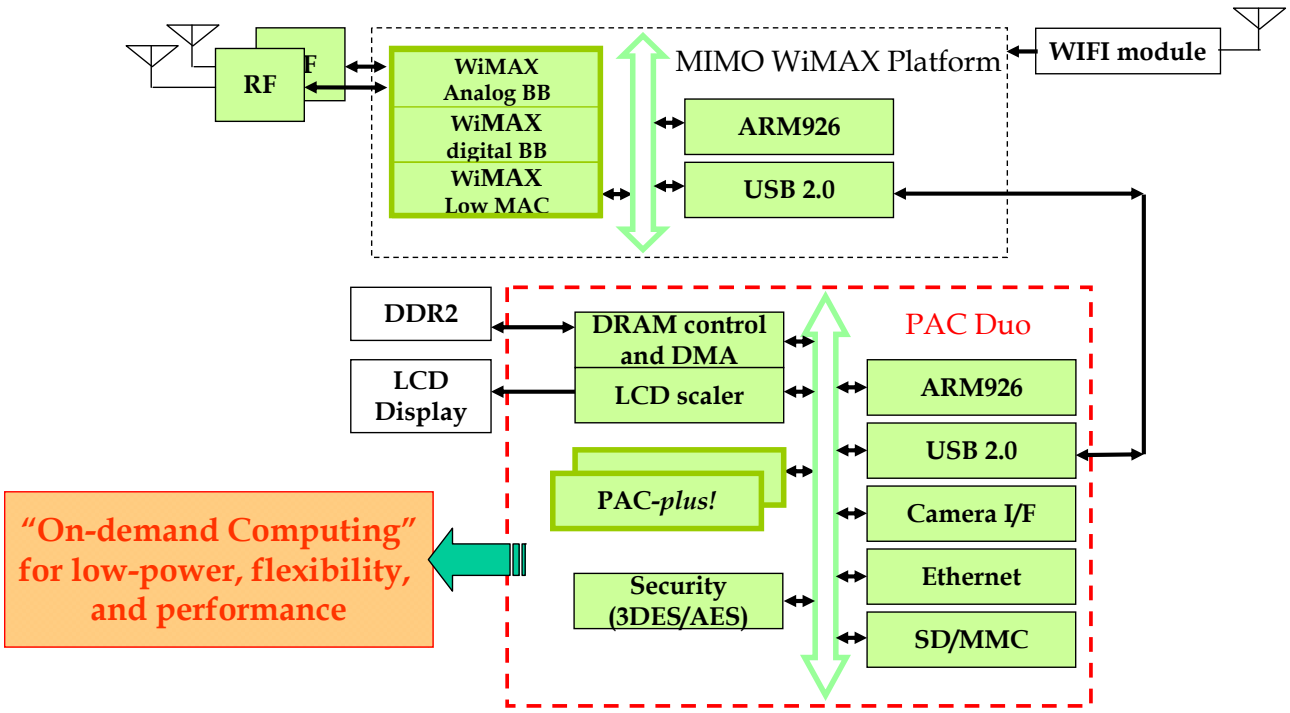
工業技術研究院
Industrial Technology
Research Institute

II. PAC-Duo SoC Architecture



工業技術研究院
Industrial Technology
Research Institute

WiMAX-ITRI System with MIMO WiMAX and PAC Duo



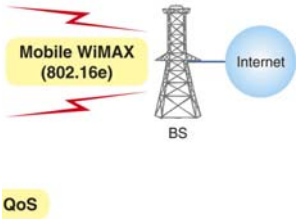
工業技術研究院
Industrial Technology
Research Institute

PAC Duo Application

- Mobile WiMAX MIMO connection
- IPTV with H.264 decoding and display
- VoIP and Web connection (Google, youtube etc)

640*480 Wi20 PMD
3-4 inch display

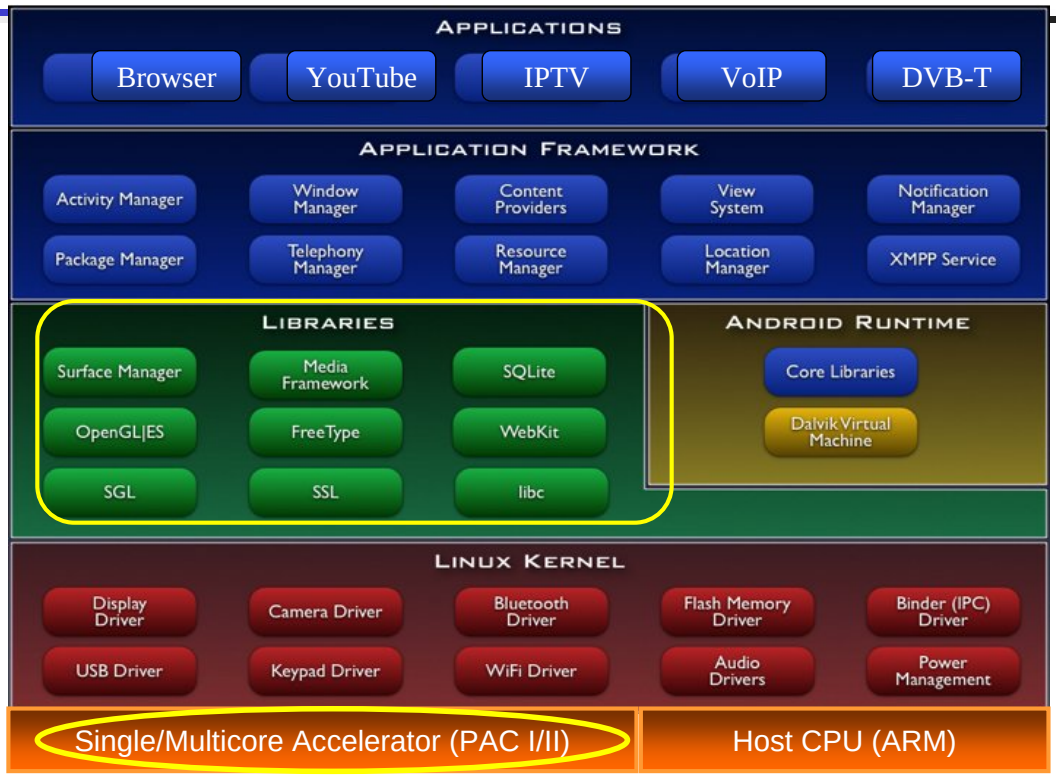
Internet connected
thin-client



Mobile WiMAX MIMO

工業技術研究院
Industrial Technology
Research Institute

III. DSP-based Accelerator for Android



工業技術研究院
Industrial Technology
Research Institute

Android Media Player

ARM Versatile Platform + PAC V3.0

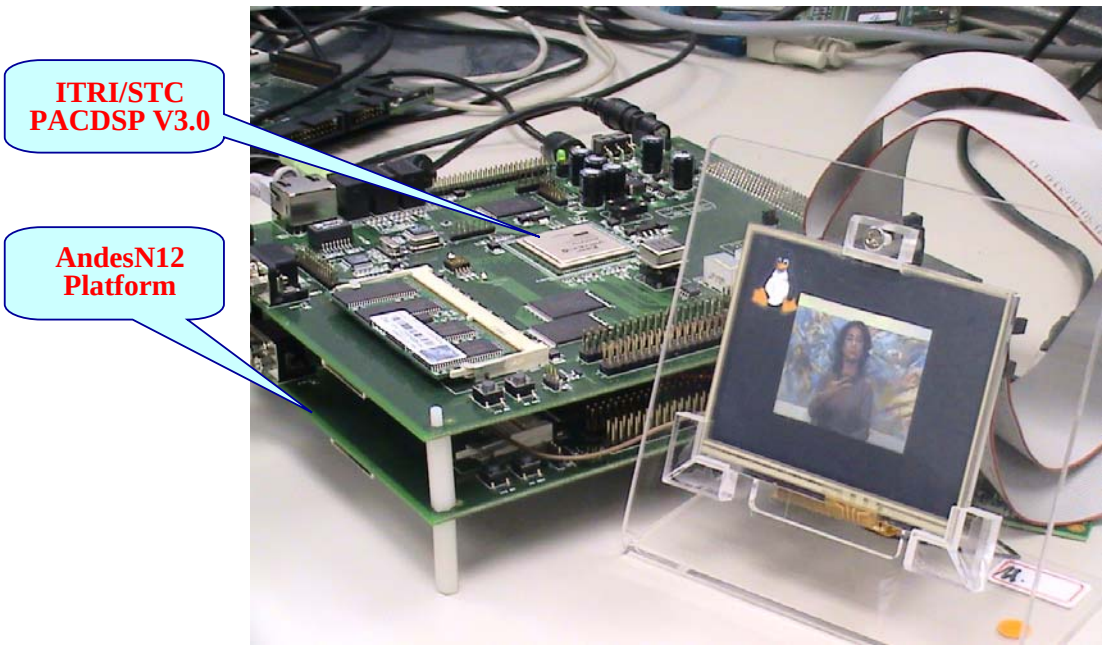
工業技術研究院
Industrial Technology
Research Institute

Demo in Computex Taipei 2008

- ITRI/STC Android SoC Prototype Demonstration in Computex Taipei 2008

工業技術研究院
Industrial Technology Research Institute

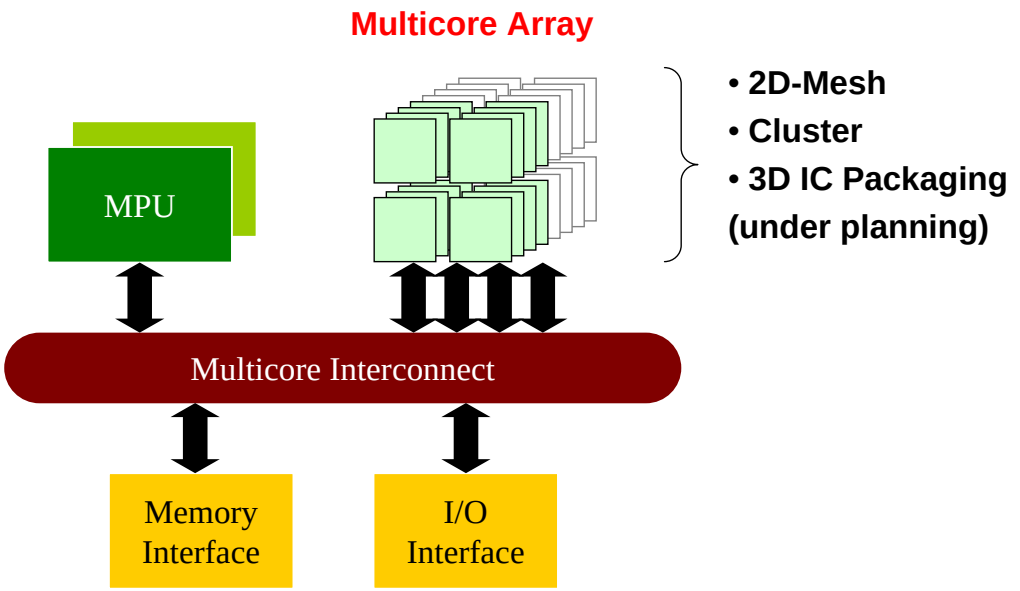
IV. Taiwan Dual-Core Platform (AndeScore & PACDSP)



FPGA Prototyping with 2 Xilinx Virtex 5 Boards

工業技術研究院
Industrial Technology Research Institute

V. Move to ITRI Multicore Architecture



工業技術研究院
Industrial Technology Research Institute

Target: Battery-powered Multicore Applications



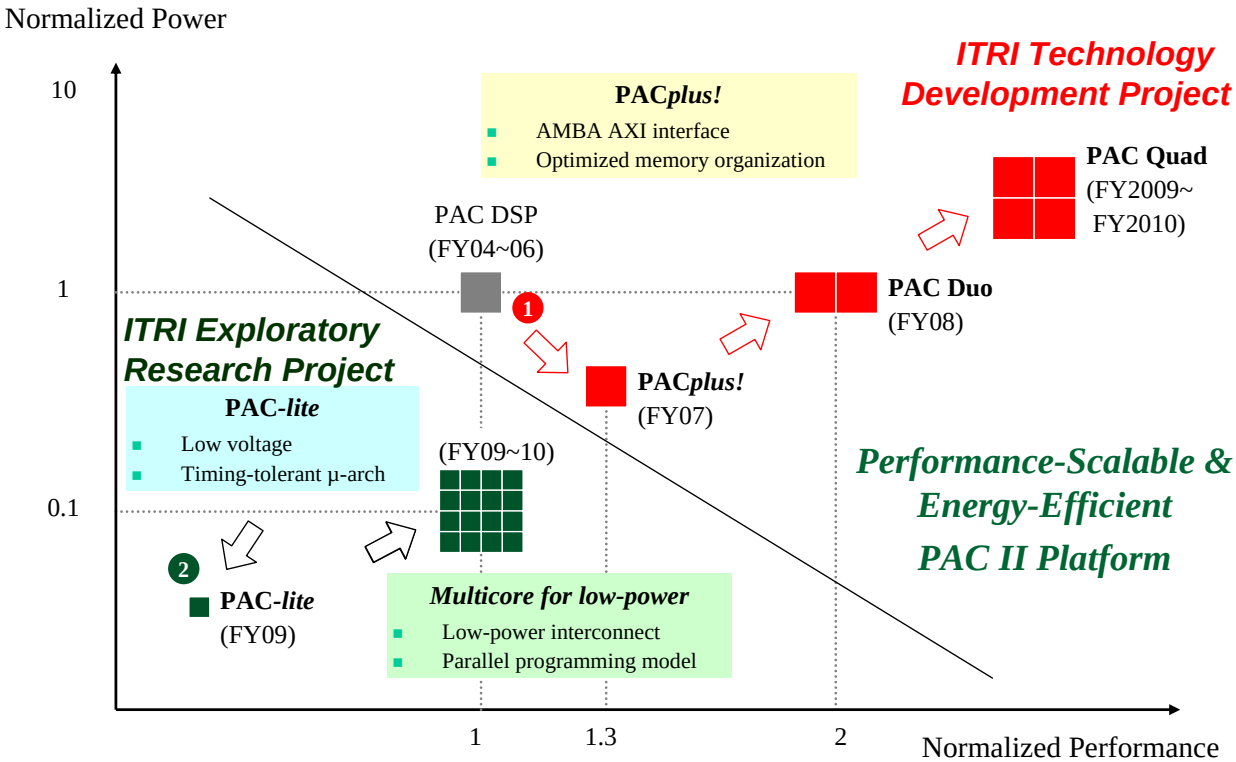
- **Intelligent robot with sense, thinking, move, vision, etc.**


- **Real-time Smart 3D image (2D photo realistic) data processing on mobile handset**


- **Smart EV cars + ITS**
- **Autonomous vehicles (MIT Angstrom project)**

工業技術研究院
Industrial Technology Research Institute

PAC Multicore Roadmap



工業技術研究院
Industrial Technology
Research Institute

Outline

- Introduction
- PAC Hardware
- Energy-Aware H.264 Decoding on PAC SoC
- PAC Phase-II Project (PAC-II)
- Conclusions

工業技術研究院
Industrial Technology
Research Institute

Conclusions

- A complete PAC DSP family is in progress
  - PAC-*plus!* predicts 30% performance improvement
  - PAC-*lite* and PAC-SIMD (for mulitcore platform) are under development for target applications
- An integrated PAC-Duo platform and SoC (2008)
  - Scalable software programming
  - Start to port Android based on dual-core SoC platform
  - Integrated with Taiwan MPU core (Andes) for Taiwan dual-core platform
- Still many open issues (SIMD, VLIW, Multicore, Architecture, Tool Chains, Software, Applications, …)
- From PAC core to next-generation ITRI Multicore research works

工業技術研究院
Industrial Technology
Research Institute

Thanks for your attention!

Acknowledgement:
Prof. Jenq-Kuen Lee and his team
for Development of PAC Tool Chain